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| 09/885,451 | 06/20/2001 | Thomas L. Ritzdorf | 291958170US02 | 3390 |

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| EXAMINER | |
|---|---|
| LEADER, WILLIAM T | |
| ART UNIT | PAPER NUMBER |
| 1742 | |

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| *Office Action Summary* | **Application No.** 09/885,451 | **Applicant(s)** RITZDORF ET AL. | |
|---|---|---|---|
| | **Examiner** William T. Leader | **Art Unit** 1742 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on 29 June 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 68-85 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 68-85 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 June 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/18/04; 11/29/02.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

## DETAILED ACTION

1. Receipt of the papers filed on June 29, 2004, is acknowledged. In response to the requirement for restriction, applicant elected Group I, claims 68-85, without traverse. Non-elected claims 86-105 were canceled.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 68-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin (6,249,055) combined with the Lowenheim text *Electroplating* and the Alkire article "Transient behavior during electrodeposition onto a metal strip of high ohmic resistance", in view of Ameen et al (US 5,685,970) and Ohmura et al (4,401,521).

5. The Dubin patent is directed to the manufacture of copper interconnects on a semiconductor wafer using a damascene technique. In discussing the background of the invention, Dubin observes that requirements for high density and performance are escalating and that these escalating requirements have been found difficult to satisfy in terms of providing a low RC (resistance capacitance) interconnect pattern, particularly when submicron vias, contacts and trenches have high aspect ratios due to miniaturization (column 1, lines 12-21). The control speed of semiconductor circuitry varies inversely with the resistance and capacitance of the interconnect pattern (column 1, lines 64-66). One way to increase the speed of semiconductor circuitry is to reduce the resistance of the conductive patterns (column 2, lines 13-14). Copper and copper alloys exhibit lower resistivity than the aluminum previously used to form interconnects (column 2, lines 52-55). Dubin also discloses that it is known to employ low dielectric constant (low K) materials as the dielectric interlayers (column 2, lines 29-31). The sequence of process steps is illustrated in figures 1-4 and figures 5-7. A dielectric layer (which may be a low K dielectric) is deposited, and vias and trenches are formed. In order to improve the corrosion resistance of copper metallization, Dubin teaches the initial deposition of a metal

layer comprising an Al or Mg alloy prior to the deposition of copper by a process such as electroplating (column 4, lines 55-61). The Al or Mg alloy may serve as a seed layer. Alternatively, a seed layer of a metal such as copper may be deposited on the Al or Mg alloy to improve nucleation and adhesion of the copper metallization (column 7, lines 40-47). After deposition of the copper, a low temperature annealing step is performed (column 4, lines 61-67).

6. Independent claims 68, 80, 82, 84 and 85 differs from the process of Dubin by reciting the use of a first current density and a second current density during the electrodeposition step. The secondary references show that in processes for electrodeposition over a seed layer it is known to begin plating at a low current density and to subsequently increase the current density. The Lowenheim text and the Alkire article provide a more theoretical approach, while the Ameen et al and Ohmura patents are directed more toward practical applications of the theory.

7. The Lowenheim text, *Electroplating*, includes a chapter directed to Plating on Nonconductors. Lowenheim states that "To electroplate on a nonconducting medium, it is necessary that the surface of that medium be made conductive in some way" (page 417). One method disclosed by Lowenheim is to form an electrically conductive seed layer by electroless deposition. Once a nonconducting surface such as a plastic has been rendered catalytic, it is ready for the deposition of electroless copper or nickel, to be followed by conventional electroplating. Lowenheim notes that since only the surface of the nonconductive plastic workpiece

where the electroless layer has been formed is conductive, and the electroless deposit is quite thin, the conductivity of the part is not comparable to that of metallic articles where the entire thickness of the article is conductive. Lowenheim teaches that "electroplating must be started at relatively low current densities to avoid burning at contact points" (page 423).

8. Lowenheim teaches that electrochemical processes follow Faraday's Laws which may be stated as follows:

> 1. The amount of chemical change produced by an electric current is proportional to the quantity of electricity that passes, and
>
> 2. The amounts of different substances liberated by a given quantity of electricity are proportional to their chemical equivalent weights.

These laws may be expressed in the form of the equation:

$$g = Iet\ /\ 96{,}500$$

where $g$ = grams of substance reacting, $I$ = current in amperes, $e$ = chemical equivalent weight, and $t$ = time in seconds. For an electrodeposition process, the grams of substance reacting is the amount metal deposited at the cathode. This equation indicates that there is a direct relationship between the thickness of material deposited and the current, and a direct relationship between the thickness of material deposited and the deposition time. There is an inverse relationship between the current applied in an electrodeposition process and the time it takes to deposit a given amount of metal. Lower current leads to longer deposition time,

while higher current results in shorter deposition times. This fundamental relationship of electrodeposition provides motivation for using higher current because it allows the process to be completed more quickly, resulting in more efficient and economical operation. See pages 12-13.

9. The Alkire article is directed to electrodeposition onto a workpiece having a high ohmic resistance. Alkire teaches that in the fabrication of printed circuit boards, a thin metal coating is initially applied to an insulating substrate by electroless deposition. This thin metal coating is a seed layer which is subsequently thickened by cathodic electrodeposition. The final deposit is usually thicker near the region of electrical contact and may be primarily attributed to the high ohmic resistance to the thin electroless deposit. Alkire develops a mathematical basis for the dependence of deposit thickness distribution on ohmic effects, mass transfer, and charge transfer. Alkire states that the method of solution is not specifically restricted to the circuit board example. See page 1935. In the conclusions section of the article, Alkire observes that the common usage of a high current density "strike" or initial plating on the electroless deposit may involve highly nonuniform deposition". See page 1940. This statement, along with the detailed mathematical discussion, suggests the use of a low initial plating current to achieve improved deposit uniformity.

10. The Ameen et al patent is cited to illustrate an application of the procedure taught by Lowenheim, and to provide additional motivation for initiating

electroplating on a seed layer at a low current density followed by higher current densities. The patent is directed to a method for metallizing polymeric films by electrodeposition. The metallized films may be used in the production of circuit boards (column 1, lines 31-36). Ameen et al teach that when the non-metallic, electrically insulating substrate is a flexible polymeric sheet, the metal, such as copper, may be electrodeposited directly on a flash of metal which has been sputtered, vapor deposited, electrolessly deposited, or adhered by similar techniques on the sheet (column 1, lines 37-41). Thus, Ameen teaches the preliminary deposition of a current-carrying metallic seed layer. Conventional electrodeposition methods for copper on polymeric sheets use current densities which result in lengthy deposition times (column 2, lines 22-26). Like Lowenheim, Ameen et al recognize that the rate of metal deposition is basically dependent on the magnitude of the current which can be applied to the metal on the substrate, and that the current is limited by the thickness as well as the current-carrying characteristics of the metal on the substrate (column 2, lines 34-40). Ameen et al teach that the problem of long deposition time can be overcome by a method in which the current applied to the substrate is increased as the deposition process is carried out. In the invention of Ameen et al, the anode electrodes opposed to the cathodic polymeric sheet to be plated are energized in groups. As metal is deposited onto the initial flash of metal on the substrate by the initial groups of anodes, the increased current carrying capacity of the thicker metal is utilized to allow subsequent groups of

anodes to have higher energization levels. The ever increasing thickness of the metal on the substrate and its increasing current-carrying capacity, is used to increase the electrodeposition rate of metal by continually increasing the current based on the current carrying capacity of the deposited metal (column 10, lines 39 – column 11, line 3). More specifically, the first group of anodes is energized at a level which the flash metal seed layer on the substrate can handle. The first group of anodes deposits metal from the electrolytic solution onto the flash metal, thereby building up the thickness of the metal on the substrate. Eventually, each group of anodes can be energized at its desired operating level (column 11, lines 4-42). It is noted that the Ameen et al patent pertains to fabrication of circuit boards. As stated above, that Alkire refers to printed circuit boards but indicates that the method of solution of the equations is not specifically restricted to the circuit board example. Similarly, one of ordinary skill in the art would recognize that the teaching of Ameen et al is applicable to workpieces other than circuit boards.

11. The Ohmura et al patent, like the Ameen et al patent, is cited to illustrate an application of the procedure taught by Lowenheim, and to provide additional motivation for initiating electroplating on a seed layer at a low current density followed by higher current densities. The patent is directed to the formation of a conductor structure by electroplating metal into openings formed in a nonconductive resist on a thin metal film. Ohmura et al recognize that uniformity of the deposit may present a problem. They state that "when the thin film

conductor pattern is directly electroplated, the thickness of the plated layer is not uniform if the length of the fine-patterned conductor structure exceeds that correspond to a resistance of 5 ohms." (column 1, lines 44-48). Additional problems include protrusions formed at a side of the conductor line and poor adhesive of the plated layer to the substrate (column 3, lines 39-51). To overcome these problems, Ohmura et al teach plating at a low current density in an initial stage of electroplating and then raising the current density (column 3, lines 52-56). Initial electroplating current density may be 0.05-2 A/dm$^2$ (0.5-20 mA/cm$^2$ using the conversion factors 1 dm$^2$ = 100 cm$^2$ and 1A = 1000mA). See column 3, lines 64-66. Subsequently current density may be in the broad range of 3-50 A/dm$^2$ (30-500mA/cm$^2$). See column 3, lines 11-19. The film thickness developed in the first electroplating stage may be 0.3-10 μm (column 3, lines 66-67). Example 1 illustrates the deposition of copper in which current density is stepped from an initial low value to a higher value.

12. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. The Lowenheim text and the Alkire article particularly demonstrate that the theoretical principles underlying the electrodeposition process are well understood and that one of ordinary skill in the art of electroplating has a knowledge of these principles and their practical application. Thus, the level of skill is considered to be high. It would have been obvious at the time the invention was made to have begun the electrodeposition step of Dubin et al at a low current

density and to have increased the current density after a period of time in which the thickness and current-carrying capacity of the plated layer had grown as taught by Lowenheim, Alkire, Ameen et al and Ohmura et al because a number of advantages resulting from the initial use of a low current density, including avoidance of burning the thin seed layer and increased uniformity of deposit, would have been obtained, and the advantage of shorter total deposition time and increased productivity would have been obtained by subsequently raising the current density. As noted above, Lowenheim and Alkire include a more theoretical presentation in which an increase of current density during electroplating is suggested, while Ameen et al and Ohmura et al illustrate actual processes in which current density is increased. All provide motivation for increasing the current density after an initial period of electroplating.

13. With respect to claim 69, the workpiece of Dubin includes recessed microstructures which would be partially filled during use of the low initial current density suggested by the secondary references.

14. With respect to claim 70, Dubin shows that the microstructures are filled indicating that the metal deposited has a grain size sufficiently small to fill the microstructures. Dubin teaches that the microstructure have a submicron dimension, overlapping the range of less than or equal to 0.3 micron.

15. With respect to claims 71 and 76, Dubin teaches that the low temperature annealing may be carried out at a temperature in the range of 150 to 450 °C

(column 5, line 11). The range recited by applicant of less than 250°C overlap the range of Dubin. The range of instant claim 76 is considered to include temperatures of 300°C of below. Choice of a value from within the range disclosed by Dubin would have been obvious.

16. With respect to claims 72-75 and 77 which relate to current density values and time of deposition, choice of these values based on the teaching of the secondary references would have been a matter of routine optimization within the skill of the art. It is noted that the values recited in the instant claims are essentially the same as those disclosed by Ohmura et al.

17. With respect to claim 78, it was stated above that Dubin discloses the use of a seed layer. Dubin explains that a seed layer is required to carry electrical current for electroplating (column 3, lines 1-3).

18. With respect to claims 81 and 83, the secondary references disclosed the application of the increased second current density immediately following the lower initial current density.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 571-272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WL
William Leader
September 19, 2004

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